EAST SEARCH

7/31/04

L#	Hits	Search String	Databases
L1	296	((electronic near2 device$1) or IC or "integrated circuit") with (test near2 (environment or setu	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	7867	((electronic near2 device$1) or IC or "integrated circuit") with (virtual or simulat$3 or emulat$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L7	212	4 and (test near2 (environment or setup))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L9	964261	((electronic near2 device$1) or IC or "integrated circuit")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	206	9 and ((test near2 (environment or setup)) with (virtual or simulat$3 or emulat$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L11	350	3 or 7 or 10	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L12	37	11 and ((input near2 signal$1) with (emulat$3 or simulat$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L13	26	11 and ((output near2 signal$1) with (evaluat$3 or measur$5))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L15	17	11 and ((test near2 (environment or setup)) with (calibrat$3 or evaluat$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L16	15	11 and ((adjust$4 or modif$4 or modification) with ((virtual or simulat$3) near2 (device or circ	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L17	10	11 and ((redesign$3 or adjust$4 or modif$4 or modification) with ((actual or electronic) near2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L19	86	11 and ((timing near2 circuit$2) or timer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L20	3	11 and (((timing near2 circuit$2) or timer) with (time near2 interval$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L22	176	11 and (tester or "test interface")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L23	59	19 and 22	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L14	59	12 or 13	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	40	1 and ((test near2 (environment or setup)) with (virtual or simulat$3 or emulat$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L18	34	15 or 16 or 17	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L21	11	11 and (((timing near2 circuit$2) or timer) with interval$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L26	15099	9 and (test near2 (system or environment or setup))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L27	229	26 and (((timing near2 circuit$2) or timer) with (time near2 interval$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L28	2	11 and (("test driver" with (input near2 signal$1)) or ("test receiver" with (output near2 signal$	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L29	105	14 or 3 or 18	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L30	2	27 and 29	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L31	14	9 and ((test near2 (system or environment or setup)) same (((timing near2 circuit$2) or timer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L32	168	27 and (((timing near2 circuit$2) or timer) with signal)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L33	57	27 and (((timing near2 circuit$2) or timer) with signal with (input and output))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L34	54	29 and 22	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L35	206	11 and (tester or (test$2 near2 interface))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L36	66	29 and 35	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L37	169	11 and (tester or (tester near2 interface))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L38	50	29 and 37	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L25	16	11 and ("test driver" or "test receiver")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L39	698	26 and (test near2 (driver$1 or receiver$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L40	333	26 and ((test near2 (driver$1 or receiver$1)) with signal)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L41	55	26 and ((test near2 (driver$1 or receiver$1)) with signal with (input and output))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L42	63	26 and (test near2 driver$1) and (test near2 receiver$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

L43	5	26 and ((test near2 driver$1) with signal with input) and ((test near2 receiver$1) with signal wi	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L44	8	11 and (test near2 driver$1) and (test near2 receiver$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

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Results of search set L29:14 or 3 or 18

Document	Kind Codes	Title	Issue Date	Current OR	Abstract
US 20040111252	A1	Method and system for emulating a design under test associated with a test environment	20040610	703/28	
US 20040088617	A1	Method and apparatus for conditioning of a digital pulse	20040506	714/724	
US 20040024577	A1	Method and system for automatic recognition of simulation configurations of an integrated circ	20040205	703/14	
US 20030217345	A1	Event based IC test system	20031120	716/6	
US 20030217343	A1	Manufacturing method and apparatus to avoid prototype-hold in ASIC/SOC manufacturing	20031120	716/4	
US 20030217341	A1	Architecture and design of universal IC test system	20031120	716/4	
US 20030158616	A1	Program conversion system	20030821	700/97	
US 20030143519	A1	Apparatus and method for evaluating tissue engineered biological material	20030731	435/4	
US 20030132768	A1	Apparatus and methods for measuring parasitic capacitance and inductance of I/O leads on a	20030717	324/754	
US 20030128042	A1	Apparatus for measuring parasitic capacitance and inductance of I/O leads on an electrical cc	20030710	324/754	
US 20030122565	A1	Apparatus and methods for measuring parasitic capacitance and inductance of I/O leads on a	20030703	324/754	
US 20030115568	A1	Method of designing, fabricating, testing and interconnecting an IC to external circuit nodes	20030619	716/15	
US 20030101395	A1	System for testing devices and method thereof	20030529	714/726	
US 20030101391	A1	System for testing multiple devices on a single system and method thereof	20030529	714/718	
US 20030076125	A1	Method and system for wafer and device level testing of an integrated circuit	20030424	324/765	
US 20030049886	A1	Electronic system modules and method of fabrication	20030313	438/106	
US 20030048256	A1	Computing device with roll up components	20030313	345/168	
US 20030034787	A1	Wafer test apparatus including optical elements and method of using the test apparatus	20030220	324/752	
US 20030009733	A1	Reduced pessimism clock gating tests for a timing analysis tool	20030109	716/6	
US 20030004663	A1	Facilitating comparisons between simulated and actual behavior of electronic devices	20030102	702/66	
US 20020194560	A1	Method of and apparatus for testing a serial differential/mixed signal device	20021219	714/724	
US 20020173926	A1	Method and system for wafer and device-level testing of an integrated circuit	20021121	702/120	
US 20020143519	A1	Virtual test environment	20021003	703/28	
US 20020143486	A1	Method and apparatus for evaluating and correcting the tester derating factor (TDF) in a test (	20021003	702/117	
US 20020095304	A1	System, method, and apparatus for storing emissions and susceptibility information	20020718	705/1	
US 20020072878	A1	Deterioration diagnostic method and equipment thereof	20020613	702/183	
US 20020040466	A1	Automated EMC-driven layout and floor planning of electronic devices and systems	20020404	716/9	
US 20020040288	A1	Method for design validation of complex IC	20020404	703/17	
US 20020039030	A1	System, method, and apparatus for product diagnostic and evaluation testing	20020404	324/750	
US 20020033706	A1	System method, and apparatus for field scanning	20020321	324/750	
US 20020002698	A1	Method for verifying the design of a microprocessor	20020103	716/4	

US 20010041972 A1	TRANSACTION CLASS	20011115	703/14
US 20010037480 A1	Dual mode test access port method and apparatus	20011101	714/727
US 20010037479 A1	Selectable dual mode test access port method and apparatus	20011101	714/724
US 20010027549 A1	Method and apparatus for testing the timing of integrated circuits	20011004	714/734
US 20010000427 A1	Method of incorporating interconnect systems into an integrated circuit process flow	20010426	333/33
US 6751759 B1	Method and apparatus for pipeline hazard detection	20040615	714/55
US 6731122 B2	Wafer test apparatus including optical elements and method of using the test apparatus	20040504	324/752
US 6721922 B1	System for electronic circuit characterization, analysis, modeling and plan development	20040413	716/1
US 6718523 B2	Reduced pessimism clock gating tests for a timing analysis tool	20040406	716/4
US 6684169 B2	Facilitating comparisons between simulated and actual behavior of electronic devices	20040127	702/66
US 6678643 B1	Event based semiconductor test system	20040113	703/14
US 6678625 B1	Method and apparatus for a multipurpose configurable bus independent simulation bus functi	20040113	702/117
US 6665826 B2	Method and apparatus for testing the timing of integrated circuits	20031216	714/718
US 6665627 B2	Method and apparatus for evaluating and correcting the tester derating factor (TDF) in a test	20031216	702/117
US 6571373 B1	Simulator-independent system-on-chip verification methodology	20030527	716/5
US 6563299 B1	Apparatus for measuring parasitic capacitance and inductance of I/O leads on an electrical cc	20030513	324/158.1
US 6539531 B2	Method of designing, fabricating, testing and interconnecting an IC to external circuit nodes	20030325	716/15
US 6523151 B2	Method for verifying the design of a microprocessor	20030218	716/4
US 6498999 B1	Method and apparatus for design verification of an integrated circuit using a simulation test be	20021224	702/120
US 6487701 B1	System and method for AC performance tuning by thereshold voltage shifting in tubbed semic	20021126	716/4
US 6434517 B1	Method and system for demonstrating simulation of a communications bus	20020813	703/21
US 6427217 B1	System and method for scan assisted self-test of integrated circuits	20020730	714/733
US 6421634 B1	Interface independent test system	20020716	703/14
US 6407572 B1	System and method for testing and evaluating a device	20020618	324/765
US 6407566 B1	Test module for multi-chip module simulation testing of integrated circuit packages	20020618	324/758
US 6370675 B1	Semiconductor integrated circuit design and evaluation system using cycle base timing	20020409	716/6
US 6360192 B2	Transaction class	20020319	703/15
US 6289476 B1	Method and apparatus for testing the timing of integrated circuits	20010911	714/718
US 6282503 B1	Logic emulation system	20010828	703/15
US 6197605 B1	Method and device for test vector analysis	20010306	438/14
US 6178533 B1	Method and system for design verification	20010123	714/739
US 6163161 A	Directed self-heating for reduction of system test time	20001219	324/760
US 6124143 A	Process monitor circuitry for integrated circuits	20000926	438/18
US 6115763 A	Multi-core chip providing external core access with regular operation function interface and pr	20000905	710/72
US 6094735 A	Speed-signaling testing for integrated circuits	20000725	714/724
US 6074426 A	Method for automatically generating behavioral environment for model checking	20000613	703/13
US 6070005 A	Logic emulation system	20000530	703/15
US 6058492 A	Method and apparatus for design verification using emulation and simulation	20000502	714/33
US 6052748 A	Analog reconstruction of asynchronously sampled signals from a digital signal processor	20000418	710/57
US 5991533 A	Verification support system	19991123	703/28
US 5923567 A	Method and device for test vector analysis	19990713	716/2
US 5920490 A	Integrated circuit test stimulus verification and vector extraction system	19990706	716/2
US 5898862 A	Method for configuring an integrated circuit for emulation with optional on-chip emulation circu	19990427	703/28

US 5841967 A	Method and apparatus for design verification using emulation and simulation	19981124	714/33
US 5798645 A	Hardware emulations system with delay units	19980825	703/15
US 5778004 A	Vector translator	19980707	714/724
US 5758123 A	Verification support system	19980526	703/22
US 5699554 A	Apparatus for selective operation without optional circuitry	19971216	716/4
US 5699283 A	Logic emulation system	19971216	703/15
US 5684721 A	Electronic systems and emulation and testing devices, cables, systems and methods	19971104	703/23
US 5633879 A	Method for integrated circuit design and test	19970527	714/738
US 5633812 A	Fault simulation of testing for board circuit failures	19970527	703/15
US 5557774 A	Method for making test environmental programs	19960917	703/21
US 5535223 A	Method and apparatus for the verification and testing of electrical circuits	19960709	714/744
US 5479355 A	System and method for a closed loop operation of schematic designs with electrical hardware	19951226	703/14
US 5477160 A	Module test card	19951219	324/755
US 5475624 A	Test generation by environment emulation	19951212	703/15
US 5414715 A	Method for automatic open-circuit detection	19950509	714/724
US 5410547 A	Video controller IC with built-in test circuit and method of testing	19950425	714/732
US 5371851 A	Graphical data base editor	19941206	345/501
US 5329471 A	Emulation devices, systems and methods utilizing state machines	19940712	703/23
US 4937827 A	Circuit verification accessory	19900626	714/33
US 4853626 A	Emulator probe assembly for programmable logic devices	19890801	324/754
US 4775831 A	In-line determination of presence of liquid phase moisture in sealed IC packages	19881004	324/664
US 4744084 A	Hardware modeling system and method for simulating portions of electrical circuits	19880510	714/33
US 4715046 A	Frequency agile signal generator for emulating communications environments	19871222	375/301
US 4381441 A	Methods of and apparatus for trimming film resistors	19830426	219/121.69
US 3781680 A	DIFFERENTIAL METHOD OF PHOTOCURRENT MEASUREMENT	19731225	324/123R
DE 10122252 A1	Testing and simulation of integrated circuits in a test bench environment using hardware and	20021121	
US 6543034 B	Multi-environment testing method of system-on-chip (SoC) integrated circuit (IC), involves sir	20030610	
US 6539341 B	Function-based tagged log information management for application specific integrated circuit	20030325	
US 6498999 B	Integrated circuit design verification apparatus using computer simulation test environment, e	20021224	
DE 10122252 A	Testing and simulation of integrated circuits in a test bench environment using hardware and	20021121	
US 20020143519 A	Test environment and actual electronic device performance evaluation method involves evalu	20021003	